

INVENTORS:

CHUI HA CHANG
JONG WOO SON
JUNG JAE KIM

THE UNIVERSITY OF CHICAGO

**PATTERNED SEED LAYER SUITABLE FOR ELECTRON-
EMITTING DEVICE, AND ASSOCIATED FABRICATION
METHOD**

5 CROSS REFERENCE TO RELATED APPLICATION

 This is related to Chang et al., co-filed U.S.
patent application Ser. No.: .attorney
docket No.: CDDC/CHC/001. To the extent not repeated
herein, the contents of Chang et al., are incorporated
10 herein by reference.

FIELD OF USE

 This invention relates to carbon based
field emitters. More particularly, this
15 invention relates to the structure and
fabrication of an electron-emitting device in
which electrically conductive seed material is
situated between electron-emissive elements, on
one hand, and emitter electrodes, on the other
20 hand, and which is suitable for use in a flat-
panel display of the cathode-ray tube ("CRT")
type.

BACKGROUND

25 A flat-panel CRT display basically consists
of an electron-emitting device and a light-
emitting device that operate at low internal
pressure. The electron-emitting device,
commonly referred to as a cathode, contains
30 electron-emissive elements that emit electrons
over a wide area.

 The emitted electrons are directed towards
light-emissive elements distributed over a
35 corresponding area in the light-emitting
device. Upon being struck by the electrons,

5 The catalyst layer 25 is normally a
conductive material that is layer 25
effectively does not electrically isolate each
group of elements 45 from each other. Thus,
there could be a kind of intercoupling of
electrons emissive elements 45 through layer
25. That means electron emission from a group
of elements 45 would have an effect on the
10 other group of element 45. A degradation of
one group of elements 45 usually means other
groups of elements 45 would have an effect on
the emitting of other groups of element 45.

15 The intercoupling of the electron emission
elements 45 also causes an undesirable process
of non-uniformity of deposition, patterning and
etching of the electron emission elements 45.
The differences in the uniformity of the
20 electron emission elements creates a situation
where the elements 45 have different threshold
voltage for electron emission. Thus, most of
elements 45 would not start to emit electrons
at the same time.

25 Because of the intercoupling provided by
catalyst layer 25, a few of the groups of the
elements 45 that would have low value of
voltage could become the primary source of
30 electron emitting for the entire group in the
display device rather than emitting electrons
from most of the groups of elements 45. Thus,
those elements 45 that act as a primary
electron emitting source could result in the
35 emitter degradation.

It is therefore desirable to have a seed layer upon which the carbon based emitter electrons can be formed and treated that reduces the number and/or complexities of steps conventionally required to fabricate the field emitter structure.

It is desirable to have a conductive seed layer that provides conductivity at selected areas along baseplate 10 but does not itself electrically interconnect these areas. In this regard, electron-emissive elements 45 at each location where one gate electrode 40 crosses over one emitter electrode 15 operate as a unit and need not be conductively coupled.

It is also desirable to configure the seed layer in such a way that underlying emitter electrodes be externally electrically accessible along their upper surfaces without the necessity of performing a separate etching operation to cut openings through the seed layer. Furthermore, it is preferable to provide a suitable pattern in the seed layer without employing any additional masking steps beyond those used for patterning other components in the field emitter.

30

GENERAL DISCLOSURE OF THE INVENTION

The present invention furnishes an electron-emitting device having a seed layer patterned to meet the foregoing needs. The present seed layer contains multiple laterally separated sections situated between electron-emissive elements, on one hand, and emitter electrodes, on the other hand. The sections of the seed layer are spaced apart along each emitter electrode.

The seed sections underlie gate electrodes of the present electron-emitting device in various ways. In one general embodiment, the seed sections are basically configured as seed strips situated below the gate electrodes. Each seed strip is sufficiently long to extend over at least one, typically all, of the emitter electrodes.

In another general embodiment of the seed layer, the seed sections are basically configured as seed portions spaced apart below each gate electrode and above each emitter electrode. As viewed in the vertical direction, the seed portions are roughly centered at the locations where the gate electrodes cross over the emitter electrodes. As contrasted to the first-mentioned embodiment in which each seed strip extends over two or more of the emitter electrodes, each seed portion in this embodiment extends over only one of the emitter electrodes.

To manufacture an electron-emitting device that employs the seed layer of the invention, a

structure is typically first provided in which a gate electrode overlies a dielectric layer that overlies an electrically seed layer overlying an emitter electrode.

5

Electron-emissive elements are situated in a composite opening extending through the gate electrode and dielectric layer in the structure so that the electron-emissive element overlies the seed layer above the emitter electrode. Creation of the seed sections involves removing portions of the seed layer located generally below spaces situated to the sides of the gate electrode.

15

Again, there is no need to perform an extra masking step to provide this initial patterning to the seed layer. The net result is that the desired pattern can be provided in the seed layer without increasing the number of masking steps.

In some applications, a separate masking step may be employed in providing the requisite pattern in the seed layer. Use of a separate masking step may arise as a matter of process convenience or due to overall processing constraints.

25

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view of the
core of a conventional electron-emitting
5 device;

Figs. 2 is a cross-sectional structural
view of the core of an electron-emitting device
provided with a seed layer patterned in
10 accordance with the invention;

Figs. 3a - 3e are cross-sectional
structural views representing steps in
manufacturing an embodiment of the electron-
15 emitting device of Fig. 2 according to the
invention; and

Fig. 4 is a cross-sectional structural view
of another embodiment of the core of an
20 electron-emitting device provided with a seed
layer patterned in accordance with the present
invention.

Like reference symbols are employed in the
25 drawings and in the description of the
preferred embodiments to represent the same, or
very similar, item or items.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the present invention, a conductive seed layer connected in series with electron-emissive elements of an electron-emitting device is patterned into multiple sections laterally separated along each emitter electrode in the device. The electron emitter of the invention typically operates according to field-emission principles in producing electrons that cause visible light to be emitted from corresponding light-emissive phosphor elements of a light-emitting device. The combination of the electron-emitting device, often referred to as a field emitter, and the light-emitting device forms a cathode-ray tube of a flat-panel display such as a flat-panel television or a flat-panel video monitor for a personal computer, a lap-top computer, or a workstation.

In the following description, the term "electrically insulating" (or "dielectric") generally applies to materials having a resistivity greater than 10^{10} ohm-cm. The term "electrically non-insulating" thus refers to materials having a resistivity below 10^{10} ohm-cm. Electrically non-insulating materials are divided into (a) electrically conductive materials for which the resistivity is less than 1 ohm-cm and (b) electrically resistive materials for which the resistivity is in the range of 1 ohm-cm to 10^{10} ohm-cm. These categories are determined at an electric field of no more than 1 volt/ μ m.

Examples of electrically conductive materials (or electrical conductors) are metals, metal-semiconductor compounds (such as metal silicides), and metal-semiconductor eutectics. Electrically conductive materials also include semiconductors doped (n-type or p-type) to a moderate or high level. The semiconductors may be of the monocrystalline, multicrystalline, polycrystalline, or amorphous type.

Electrically resistive materials include (a) metal-insulator composites such as cermet, (b) certain silicon-carbon compounds such as silicon carbide and silicon-carbon-nitrogen, (c) forms of carbon such as graphite, amorphous carbon, and modified (e.g., doped or laser-modified) diamond, and (d) semiconductor-ceramic composites. Further examples of electrically resistive materials are intrinsic and lightly doped (n-type or p-type) semiconductors.

A transverse profile is a vertical cross section through a plane perpendicular to the length of an elongated region. The row direction in a matrix-addressed field emitter for a flat-panel display is the direction in which the rows of picture elements (pixels) extend. The column direction is the direction in which the columns of pixels extend and runs perpendicular to the row direction.

Fig. 2 illustrates the core of a matrix-addressed field emitters that contain an emitter conductor patterned into conductor

strips in a vertically aligned manner according to the invention. The cross sections of Fig. 2 is taken through perpendicular planes.

5

The field emitter of Fig. 2 is created from a flat electrically insulating baseplate (substrate) 100 typically consisting of glass having a thickness of approximately 1 mm. To
10 simplify the pictorial illustration, baseplate 100 is shown in the perspective view of Fig. 2.

A patterned electrically conductive seed layer 120 is disposed on a resistor layer 115
15 which is in turn disposed on the emitter electrode 110. The seed layer 120 provides a seed platform on which the electron emission elements of the present invention are built.

20 In one embodiment of the present invention, the patterned strips of seed layer 120 are typically aligned with the gate layer 130 and situated in openings 145 in a way to isolate groups of the electron emission elements 140
25 from each other. Isolating the group of electron emission elements ensures that a defect in one group does not affect the emission quality of the other groups.

30 Fig. 3A depicts a partial cross-sectional representation of the field emitter structure 1 of one embodiment of the present invention. The method fabricating the field emitter structure 1 generally includes providing a base
35 plate 100 and disposing thereon a plurality of emitter electrodes. The group of generally

parallel emitter electrodes 110 are situated on baseplate 100.

Emitter electrodes 110 extend in the row
5 direction and constitute row electrodes. As shown in Fig. 3A, each emitter electrode 110 has a transverse profile roughly in the shape of an upright isosceles trapezoid. This profile helps improve step coverage of layers
10 formed above emitter electrodes 110.

Emitter electrodes 110 typically consist of aluminum, molybdenum, or chromium, or an alloy
15 of any of these metals. In the case of aluminum, emitter electrodes 110 are typically 0.1 - 0.5 μm in thickness.

In one embodiment of the present invention, the emitter electrode 110 is deposited in-situ
20 by a number of well known deposition methods of the prior art. In one embodiment. Sputter deposition may be used. In another embodiment, a form of evaporation deposition may be used.

Upon deposition of the emitter electrode
25 110, a photo-resistive material (PR) is coated on the emitter electrode 110. The photo-resistive coating is then soft baked. After coating and baking, the photo-resistive
30 material is exposed according to a designed patterned and developed. After developing the photo-resist material, the photo-resist material is hard baked and the part of the emitter electrode which is opened through the
35 PR after being developed is etched away and stripped away.

5 The emitter electrode 110 is patterned by a number of photolithographic processes well known in the art accordingly. Applicable etching methods include wet etching. Remaining PR maskant is stripped off by methods well known in the art.

10 Fig. 3B depicts a partial cross-sectional representation of structure 1 having undergone further steps of deposition of a resistor layer 115. The resistor layer 115 is then fabricated by deposition of a layer of resistive material on the emitter electrode layer 110 and
15 remaining surfaces of the glass 100 uncovered by the emitter electrode 110 material.

20 In one embodiment of the present invention, the resistor layer 115 is deposited by a number of well known methods in the art. In one embodiment, deposition of the resistor layer 115 is accomplished by plasma enhanced chemical vapor deposition (PECVD) method.

25 Upon deposition of the resistor layer 115, a photo-resistive material(PR) is coated on the resistor layer 115. After coating, the PR is soft baked, exposed and developed. The PR is subsequently hard baked and dry etched to
30 conform to the contours of the surface of the glass 100. Remaining PR maskant is stripped by methods well known in the art.

35 Fig. 3C depicts a partial cross-sectional representation of structure 1 having undergone further steps of depositing a conductive seed

layer 120. After coating, the PR is soft baked and exposed. The PR is subsequently developed by hard baking and wet etching to conform to the contours of the surface of the glass 100.

5 Remaining PR maskant is stripped by methods well known in the art.

In one embodiment of the present invention, the seed layer 120 is wet etched by applying a
10 combination of phosphoric acid, nitride acid, acetic acid and water.

Fig. 3D depicts a partial cross-sectional representation of structure 1 having undergone
15 further steps of depositing a dielectric layer 125. As shown in Fig. 3D, a blanket dielectric layer is formed on the surface of the conductive seed layer 120 and the resistor layer 115 covering portions of the resistor
20 layer 115 that are left uncovered by the seed layer 120.

A group of generally parallel gate electrodes 130 overlie dielectric strips 125
25 above conductive strips 120. Each gate electrode 130 lies on the entire top surface of a corresponding one of dielectric strips 125 and, accordingly, fully overlies underlying conductive strip 120. Due to the
30 characteristics of the etch procedures typically used to define the longitudinal side edges of strips 120 and 125, each gate electrode 130 may be slightly wider or narrower than underlying dielectric strip 125.

35

Fig. 3E depicts a partial cross-sectional representation of structure 1 having undergone further steps of depositing a blanket passivation layer 135. The passivation layer 135 is disposed on the gate layer 130 and portions of the dielectric layer 125 uncovered by the gate layer 130.

The passivation layer 135 overlies the entire top surface of a corresponding one of gate layer strips 130 and, accordingly, fully overlies underlying conductive seed strip 120. In one embodiment of the present invention, passivation layer 135 may be silicon dioxide (SiO_2), or silicon nitride (SiNx), or a mixture of these compounds with a SiNx . The passivation layer 135 is subsequently masked by a PR masking agent masking the passivation layer according to a designed pattern.

After masking, the passivation layer 135 and dielectric layer 125 are etched by a dry etching method, known in the art. Remaining PR is stripped.

Fig. 3F depicts a partial cross-sectional representation of structure 1 having undergone further steps of etching the structure to create cavities for depositing the electron emission elements 140.

After depositing the passivation layer 135, the passivation layer 135, and the dielectric layer 125 are etched to create cavities or

composite openings 145 for the formation of the carbon nano-tube emitters of the present invention.

5 A patterned dielectric layer consisting of a group of laterally separated generally parallel strips 125 overlying the conductive strips 120 is formed.

10 Each dielectric opening overlies a corresponding one of conductive strips 120. The longitudinal side edges of each dielectric strip 125 are in approximate vertical alignment with the longitudinal side edges of
15 corresponding seed strip 120.

In one embodiment of the present invention, the dielectric strips 125 comprises two layers of silicon dioxide and silicon nitride having a
20 thickness of 0.5 - 2.0 μm . In another embodiment, dielectric strips 125 comprise of a single layer of silicon-oxy-nitride having a thickness of 0.5 - 2.0 μm .

25 The patterning of the seed layer 120 to form strips is typically performed with one or more wet etchants depending on the constituency of layer 120.

30 Gate electrodes 130 may be configured in various ways. For example, each electrode 130 can be implemented as a main gate portion and one or more thinner adjoining gate portions as described below in connection with Fig.2

35

through the underlying portions of all seed strips 120 to underlying emitter electrode 110. On the other hand, the sets of elements 140 in each row of the electron-emissive-element sets are electrically coupled through portions of underlying conductive strip 120 respectively to all of emitter electrodes 110.

The electron-emissive elements 140 are typically filaments in shape, as depicted in Fig. 2. In this case, the principal constituent of elements 140 is typically carbon. Elements 140 can be shaped differently, for example, as cylindrical. Dielectric openings 145 may then be shaped differently from what is generally indicated in Fig. 2.

During field emitter operation, an anode in the light-emitting device (not shown here) situated opposite elements 140 draws the extracted electrons towards light-emissive elements located close to the anode. As electrons are emitted by each activated electron-emissive element 140, a positive current flows through underlying seed strip 120 to underlying emitter electrode 110.

Seed strips 120 provide the field emitter with electron-emission uniformity and short circuit protection. Strips 120 limit the number of electrons emitted by activated elements 140. Strips 120 further prevent electron emission through just a limited number of the electron

emission elements 140. This is caused by the electrical isolation of the seed layer 120.

5 This prevents some of elements 140 from providing many more electrons than other of elements 140 at the same extraction voltage and thus prevents undesirable bright spots from occurring on the viewing surface of the flat-panel display.

10 Also, if one of gate electrodes 130 becomes electrically shorted to underlying seed strip 120 and thus becomes electrically coupled to underlying emitter electrode 110, seed strip
15 120 at the short circuit location significantly limits the current flowing through the short circuit connection. With proper electron-emitter design, the presence of the short circuit does not detrimentally affect the
20 operation of any of the other sets of electron-emissive elements 140.

Such a short circuit can arise by way of a conductive path created through a dielectric
25 strip 125 or by having one or more of electron-emissive elements 140 come into contact with their gate electrode 130. In the case of a gate-electrode-to-electron-emissive-element short circuit, each shorted electron-emissive
30 element 140 is normally defective.

However, the seed strips 120 limit the current through each shorted elements 140 sufficiently that non-shortcd elements 140 in
35 that set of electron-emissive elements may still operate in the intended manner. Seed

strips 120 thus normally enable a set of
electron-emissive elements 140 containing a
small percentage of shorted elements 140 to
perform the intended electron-emitting function
5 in an adequate manner. Electron-emission
uniformity is substantially maintained.

Fig. 4 illustrates the core of a matrix-
addressed field emitters that contain an
10 emitter conductor patterned into conductor
strips in a vertically aligned manner according
to the invention. The cross sections of Fig. 4
is taken through perpendicular planes.

15 The field emitter of Fig. 4 is created the
same way as the structure in Fig. 2. However,
the patterned electrically conductive seed
layer 120 is patterned in a way so that the
20 seed strips symmetrically over-align with the
gate electrode 130. Symmetrically over-aligning
the seed strips 120 with the gate electrode 130
reduces undesirable electron emission in the
structure 1.

25 The electron emitters produced according to
the invention can be employed to make flat-
panel devices other than flat-panel CRT
30 displays. Likewise, the present electron
emitters can be used as electron sources in
products other than flat-panel devices.
Various modifications and applications may thus
be made by those skilled in the art without
35 departing from the true scope and spirit of the
invention as defined in the appended claims.